MINGJUN WANG

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EDUCATION

The Chinese University of Hong Kong 2025 – Present
Ph.D. Student in Computer Science & Engineering *Hong Kong SAR, China*

- Advisor: Prof. Bei Yu, Department of Computer Science and Engineering, CUHK
- Research Focus: AI4EDA, Circuit Representation Learning, 3D IC Design Automation

University of Chinese Academy of Sciences & ICT, CAS 2022 – 2025
Master's in Electronic Information *GPA: 3.78/4.0 (Rank: Top 5%)*

- Advisors: Prof. Xiaowei Li and Prof. Huawei Li, State Key Laboratory of Processors, Institute of Computing Technology, CAS
- Selected Courses: Deep Learning (92), Pattern Recognition (90), VLSI Testing (90)

Peking University 2018 – 2022
Bachelor's in Microelectronics Science and Technology *Beijing, China*

- Selected Courses: Neural Computation (94), Intelligent Computing Systems (100)
- Undergraduate Thesis: True Random Number Generator Based on RRAM

RESEARCH INTEREST

I am broadly interested in circuit representation learning and artificial intelligence for electronic design automation (AI4EDA) and 3D IC designs, focusing on developing novel multi-modal circuit understanding systems and neural architectures for EDA problems. My work studies how to represent circuits across RTL, netlists, physical layouts, timing, power, and verification signals, with cross-stage knowledge distillation and task-oriented circuit data as core methodologies. Meanwhile, I have solid experience in fault simulation acceleration and functional safety analysis for circuit verification. My research spans cutting-edge AI applications in 3D IC EDA and fundamental circuit verification methodologies that remain useful under real industrial design constraints.

PUBLICATIONS

Conference Papers

- *Distill3D: Cross-Stage Knowledge Distillation for Early-Stage 3D IC Timing Prediction*
  M. Wang, L. Zou, F. Gu, Y. Lu, B. Han, J. Mu, H. Li, B. Yu
  International Conference on Computer-Aided Design (ICCAD), 2026
- *CircuitNet 3.0: A Multi-Modal Dataset with Task-Oriented Augmentation for AI-Driven Circuit Design*
  M. Wang, Y. Wen, Y. Lu, F. Liu, Y. Zhao, B. Han, J. Mu, Y. Lin, R. Wang, H. Li, B. Yu
  International Conference on Learning Representations (ICLR), 2026
- *ATLAS: Asynchronous Topological Learning for Accurate FIT Prediction via Decoupled Graph Neural Networks*
  Y. Liu[†], **M. Wang**[†], S. Pei, Y. Lu, Z. Liu, B. Han, H. Li, S. Wang
  Design Automation Conference (DAC), 2026
- *AnalogVerifier: A Neuro-Symbolic Framework for Analog Circuit Verification*
  Y. Liu[†], **M. Wang**[†], P. Xu, R. Fu, B. Yu, T.-Y. Ho
  International Conference on Machine Learning (ICML), 2026
- *LibPilot: Knowledge-Constrained Dual-Agent Reasoning for Standard Cell Library Tuning*
  Y. Liu, Z. Cheng, **M. Wang**, R. Fu, C. Wang, B. Yu
  International Conference on Computer-Aided Design (ICCAD), 2026
- *ChatFCM: Comprehension-Synthesis Decoupling for LLM-Based Functional Coverage Model Generation*
  Y. Pu, Y. He, Z. Chen, **M. Wang**, B. Yao, Z. Lin, Q. Chen, B. Li, S. Chen, Z. He, W. Yu, Y. Li, B. Yu
  International Conference on Computer-Aided Design (ICCAD), 2026

[†] Equal contributors.

- *LLM-Assisted Circuit Verification: A Comprehensive Survey*
  H. Liu, Y. Lu, **M. Wang**, X. Yao, B. Yu
  Asia and South Pacific Design Automation Conference (ASP-DAC), 2026
- *Bridging Layout and RTL: Knowledge Distillation based Timing Prediction*
  M. Wang, Y. Wen, B. Sun, J. Mu, J. Li, X. Wang, J. Ye, B. Yu, H. Li
  International Conference on Machine Learning (ICML), 2025 **(Spotlight)**
- *VIRTUAL: Vector-based Dynamic Power Estimation via Decoupled Multi-Modality Learning*
  Y. Lu[†], **M. Wang**[†], Y. Wen, B. Han, J. Mu, H. Li, B. Yu
  International Conference on Computer-Aided Design (ICCAD), 2025
- *MOSS: Multi-Modal Representation Learning on Sequential Circuits*
  M. Wang, B. Sun, J. Mu, F. Gu, B. Han, T. Yang, X. Zhang, S. Liu, Y. Wen, H. Wang, J. Gao, Z. Chao, H. Han, Z. Liu, S. Liang, J. Ye, B. Yu, X. Li, H. Li
  Design Automation Conference (DAC), 2025
- *EPICS: Efficient Parallel Pattern Fault Simulation for Sequential Circuits via Strongly Connected Components*
  M. Wang, H. Wang, J. Mu, X. Zhang, B. Sun, Y. Wen, Z. Liu, F. Gu, J. Gao, S. Liang, J. Ye, X. Li, H. Li
  Design Automation Conference (DAC), 2025
- *DFTS: An Efficient Design-for-Test Flow for Scan Design*
  J. Gao, **M. Wang**, J. Liu, W. Li, Z. Liu, J. Ye, H. Li
  International Symposium of EDA (ISEDA), 2025
- *ETPG: Efficient Transition Fault Simulation via Dual-Strategy Pattern Parallelism and Gate Restructuring*
  M. Wang, H. Wang, Z. Liu, F. Gu, J. Mu, J. Tang, J. Gao, H. Li, J. Ye, X. Li
  Asia and South Pacific Design Automation Conference (ASP-DAC), 2025 **(Best Paper Nomination)**
- *DDP-Fsim: Efficient and Scalable Fault Simulation for Deterministic Patterns*
  F. Gu, **M. Wang**, J. Mu, Z. Liu, J. Tang, H. Wang, Y. Wang, J. Ye, H. Li, X. Li
  International Conference on Computer-Aided Design (ICCAD), 2024 **(Best Paper Nomination)**
- *Efficient Functional Safety Method for Gate-Level Fine-Grained Digital Circuits with ISO-26262*
  M. Wang, H. Wang, J. Mu, Z. Liu, J. Gao, J. Ye, H. Li, X. Li
  International Test Conference in Asia (ITC-Asia), 2024

Journal Papers

- *Bit-Compressed Concurrent Fault Simulation with Efficient Fault List*
  F. Gu, Z. Chao, H. Wang, J. Mu, **M. Wang**, J. Gao, Y. Wang, J. Ye, X. Li, H. Li
  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Early Access, 2026
- *DomSim: Hardware-Aware Hybrid Fault Simulation Approach with Dominator Tree-guided Partitioning*
  M. Wang, H. Wang, F. Gu, Z. Liu, J. Mu, S. Liang, Z. Yu, Z. Liang, J. Gao, J. Tang, J. Ye, B. Yu, X. Li, H. Li
  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2025

Research Experience and Projects

AI4EDA, Multi-Modal Circuit Data, and 3D IC EDA Flow Automation May 2024 – Present

Department of Computer Science and Engineering, CUHK

- Built comprehensive multi-modal circuit datasets incorporating specification, RTL, netlist, layout, timing, and power data; supported large-scale benchmarking for AI-driven EDA research.
- Developed learning-based methods for circuit representation, cross-stage PPA prediction, and flow-oriented 3D IC design automation, with results published at ICLR 2026, ICML 2025 (Spotlight), and ICCAD 2025.
- Implemented automated pipelines for circuit representation extraction and timing/power knowledge distillation across design stages.

Fault Simulation Research Jul. 2023 – Mar. 2025

State Key Laboratory of Processors, ICT, CAS

- Developed hardware-aware and parallel fault simulation frameworks for large-scale digital circuits, covering deterministic-pattern, transition-fault, and sequential-circuit settings.
- Proposed novel optimization techniques (dominator-tree partitioning, SCC-aware decomposition, dual-strategy pattern parallelism) for scalable circuit verification and design-for-test workflows.
- Research outcomes were published as IEEE TCAD journal articles and multiple top-tier conference papers at DAC, ASP-DAC, ICCAD, and ITC-Asia.

Industrial Experience – CASTEST Sep. 2021 – Jan. 2025

Beijing, China

- Contributed to the development of digital circuit fault simulation platforms and functional safety analysis tools.
- Worked on ISO 26262-oriented workflows for automotive-grade chips, strengthening a practical view of industrial EDA flow requirements.
- Engaged in commercial EDA tool development cycles spanning requirement engineering and deployment for industrial users.

True Random Number Generator Based on RRAM Sep. 2020 – Jun. 2022

Undergraduate Thesis Project, Peking University

- Designed and implemented an RRAM-based true random number generator with stable entropy extraction.
- Evaluated randomness quality using the NIST SP 800-22 statistical test suite.

Awards and Honors

Winner, IEEE ICLAD-DAC GenAI Hackathon, 2025.

Second Place, EDAthon 2025, Programming Competition on Electronic Design Automation (Awarded by IEEE CEDA).

Second Prize (Enterprise Track), The 8th China Graduate IC Innovation Contest, 2025.

International Exchange Scholarship for Empowerment, 2025 (Awarded by Institute of Computing Technology, CAS).

Director's Special Award, 2024 (1st out of 400 students, awarded by Institute of Computing Technology, CAS).

National Scholarship, 2024 (Top 2% of students nationwide).

Special Prize, LLM4EDA Summer School Hackathon, 2024 (1st out of 100 participants, awarded by National Key Laboratory of Integrated Chips and Systems).

Academic Endeavor Award, 2024 (Awarded by the EDA Elite Challenge for research excellence).

First Prize of Academic Scholarship, Chinese Academy of Sciences, 2024 (Top 15% of students in CAS).

First Prize, EDA^2 Integrated Circuit Elite Challenge, 2023 (1st out of 230 teams, awarded by Huawei HiSilicon).

Huawei Intelligent Base Scholarship, 2023 (Awarded to top 5% of students by Huawei Technologies).

Cambricon Outstanding Student Award, 2023 (Awarded to 10 / 300 students by Cambricon Technologies).

Outstanding Contribution Award for Beijing 2022 Winter Olympics, 2022 (Top 10% of volunteers in PKU).

Peking University Social Work Award, 2019, 2020 (Awarded for exceptional contributions to social work).

Leadership and Volunteer Work

Volunteer Leader, Beijing 2022 Winter Olympics Oct. 2021 – Mar. 2022

International Olympic Committee

- Served as Olympic Family Assistant (OFA), managing VIP reception, scheduling, and transport arrangements.
- Contributed to 500-day preparation work, including event coordination, promotional design, and volunteer management.

President, Student Science and Technology Association Sep. 2023 – Dec. 2024

Institute of Computing Technology, CAS

- Organized 16 science popularization sessions covering fundamental computer science topics.
- Promoted the "Spring Equinox Science Program," boosting students' interest in technology.

Deputy Secretary-General, PKU Student Activity Center Oct. 2020 – Apr. 2022

Peking University

- Organized university-wide events, including volunteer commendation galas and Winter Olympics volunteer recruitment campaigns.

Skills

Programming: Verilog, SystemVerilog, Python, C++, etc.
EDA Tools: Synopsys VCS, Design Compiler, Cadence Xcelium, etc.
Frameworks: PyTorch, TensorFlow
Specialized Knowledge: AI4EDA, 3D IC Design Automation, Circuit Representation Learning, Fault Simulation, ISO 26262 Functional Safety
Others: Git, Linux, LaTeX